

AD-A253 846



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QUARTERLY PROGRESS REPORT NUMBER 2

1 January 1992 - 31 March 1992

Sponsored by

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MDA 972-91-C-0034

Submitted by

Georgia Tech Research Institute
Georgia Institute of Technology
Atlanta, Georgia 30332-0420

Effective Date: 16 September 1991

Expiration Date: 30 March 1993

Contract Amount: \$568,572

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FIELD EMISSION CATHODE AND VACUUM
MICROELECTRONIC MICROWAVE AMPLIFIER
DEVELOPMENT

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I. EXECUTIVE SUMMARY

- Upgraded composite growth facility in place and first composite material growth runs accomplished
- Upgraded emitter array fabrication facility for modified fabrication processing designed and in procurement/fabrication
- New integrated laboratory facility in Microelectronics Research Center for fabrication and testing
- Automated emission test equipment designed and specified for procurement and assembly
- Initial mask set complete for new photolithography based fabrication process completed
- Array capacitance modelling begun, initial results obtained and significant insight to effects of geometrical and materials variables being developed

Statement A per telecon
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II. MILESTONE STATUS

A -- Field Emitter Cathode Development

A.1. Composite Development

A.1.a. Increase composite ingot volume and die size

Start -- 1 October 91 Planned

1 October 91 Actual

Completion -- 31 March 93 Planned

A.1.b. Optimize composite growth morphology

Same as A.1.a.

A.2. Emitter Tip Geometry and Composition

A.2.a. Etching studies

Start -- 1 November 91 Planned

1 November 91 Actual

Completion -- 31 March 93 Planned

A.2.b. Emitter coatings

Start -- 1 April 92 Planned

A.3. Field Emitter Structure Development

A.3.a. Emitter ballasting

Start -- 1 April 92 Planned

A.3.b. Insulator film studies

Start -- 1 December 92 Planned

1 December 92 Actual

Completion -- 31 December 92 Planned

A.3.c. Double-deposition geometry studies

Start -- 1 December 92 Planned

1 December 92 Actual

Completion -- 31 March 93 Planned

A.4. Field Emitter Array Testing

A.4.a. Test package development

Start -- 1 November 91 Planned

1 December 91 Actual

Completion -- 31 October 92 Planned

DC and rf evaluation

Start -- 1 February 92 Planned

1 July 92 Rescheduled

Completion -- 31 March 93 Planned

A.4.b. Beam analysis

Start -- 1 April 92 Planned

Completion -- 31 March 93 Planned

III. TECHNICAL PROGRESS

A -- Field Emitter Cathode Development

A.1. Composite Development

The facilities for composite growth have been upgraded with improved cooling facilities which are planned to provide improved control of post-solidification cooling, a critical consideration in reducing the problems of cracking in the composite and enlarging the available material (die) size.

Several hot-pressing runs have been performed to provide an initial supply of the required feed material for the composite growth operations.

Two composite growth runs have been made, the first of which has been judged, preliminarily, to have been successful, and the second of which failed as a result of difficulties with the density of the feed material. The ingot from the first run is in the process of detailed characterization, which requires extensive sectioning (via low speed diamond sawing), grinding, polishing, and inspection by optical and scanning electron microscopy. The sliced material is also probed electrically to evaluate tungsten fiber continuity.

A.2. Emitter Tip Geometry and Composition

The etching facility has been completed and updated to improve temperature and composition control of the phosphoric acid etch which is utilized for selective etching of the zirconia matrix material.

Initial etching development is awaiting availability of composite material from the growth operations.

A.3. Field Emitter Structure Development

This work has been started with a modelling effort to provide insight into the effects of geometrical and materials variables on emitter array capacitance. Initial results from this effort indicate that the dielectric constants of the insulator layer and composite matrix material play little or no role in determining the capacitance, and that the insulator layer thickness, when varied from 2 to 6 microns, has essentially no effect on capacitance. There is some evidence that thinner insulator layers may lead to increasing capacitance, and modelling efforts are continuing to study this aspect.

The influence of the gate aperture diameter and gate film thickness have been evaluated for a limited range of dimensions, and results to date show that these

dimensions are instrumental in determining device capacitance.

As a result of the modeling efforts, the original concept of fabrication, incorporating the double-deposition technique, will not be followed initially. It appears that thin insulator layers of less than one micron in thickness, leading to gate aperture diameters of about 0.75 microns or less, provide a simpler means of obtaining improved emitter geometries. This may allow avoidance of the complexity associated with the double-deposition concept, while minimizing operating voltages and improving transconductance.

The improved design of the vapor deposition facilities required for emitter array fabrication has been completed, and all necessary components are on order or being fabricated in house. The basic system, including all vacuum components and process control instrumentation, is in place. Several aspects of fabrication have been modified from the practice used in previous work at Georgia Tech in order to meet the requirements of the present effort. These changes have resulted in substantial differences in sample geometry, size and requirements for fixturing and heating during deposition. The initial designs for these modifications are complete and hardware is being fabricated.

A major change in fabrication practice involves the use of photolithography to define emitting areas of precise and repeatable geometry and size. The appropriate mask set (3 masks) has been designed and fabricated, and awaits completion of the deposition apparatus for initial evaluation. This fabrication procedure will provide 16 individually addressable emitting areas, each with an area of 0.1mm^2 , on a $3\text{mm} \times 3\text{mm}$ chip of composite material. It is envisioned that nine chips, in a 3×3 array, will be processed as a single die once the composite material is available in $1\text{cm} \times 1\text{cm}$ die sizes.

A.4. Field Emitter Array Testing

To take maximum advantage of the ability to fabricate large numbers of individual emitting areas, as described above, a substantial modification of testing capability is in process. A completely automated data-acquisition system has been designed, and necessary components are presently being specified. An existing ultra-high-vacuum system will be used for this work, providing a clean, cryo-pumped environment.

It is planned to use a TO-type header package for mounting of the emitter chips for testing. Evaluation of the ability to die bond the individual chips onto

standard headers using low melting material, such as indium, is planned, and will be verified in the near future.

IV. FISCAL STATUS

Expenditures this quarter	\$84,681.80
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Total expenditures to date	136,352.42
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Projected expenditures:

4/92 - 6/92	\$81,500.00
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7/92 - 9/92	\$119,600.00
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Total Projected Cost for FY92	\$337,452.00
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V. PROBLEM AREAS

- Substantial delay has been encountered in refurbishing and/or redesigning and modifying process equipment.

- Initial results from composite growth runs indicate that a solution to the cracking problems and 1cm^2 area samples are not currently realizable. Sample handling for emitter fabrication will be modified accordingly to allow studies to commence in the near term.

VI. VISITS AND TECHNICAL PRESENTATIONS

1. "A Model to Determine the Effect of Emitter Geometry on the Capacitance of the Low Voltage Field Emitter Array"
D.N. Hill, W.L. Ohlinger and R.K. Feeney, presented at the 1992 Tri-Service/NASA Cathode Workshop, Greenbelt, Maryland, March 17-19, 1992.